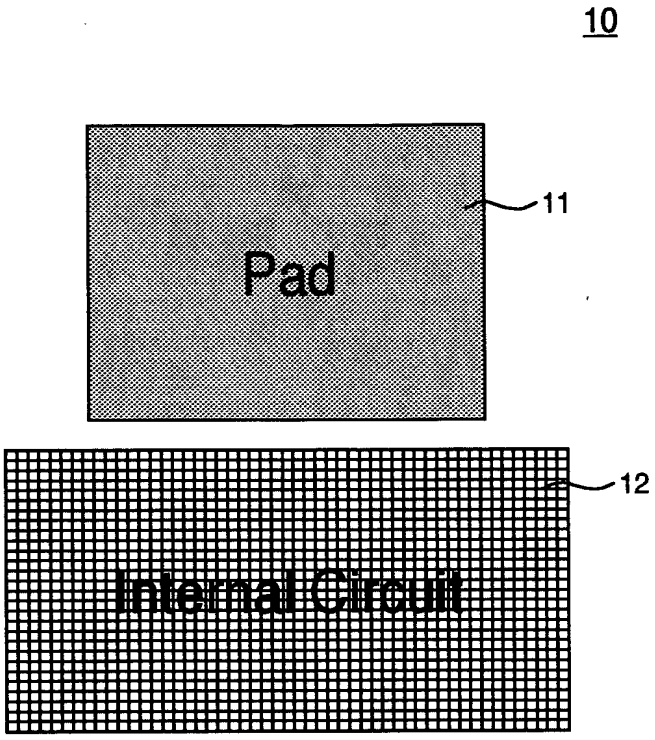


Top side view

(Conventional Art)

Fig. 1

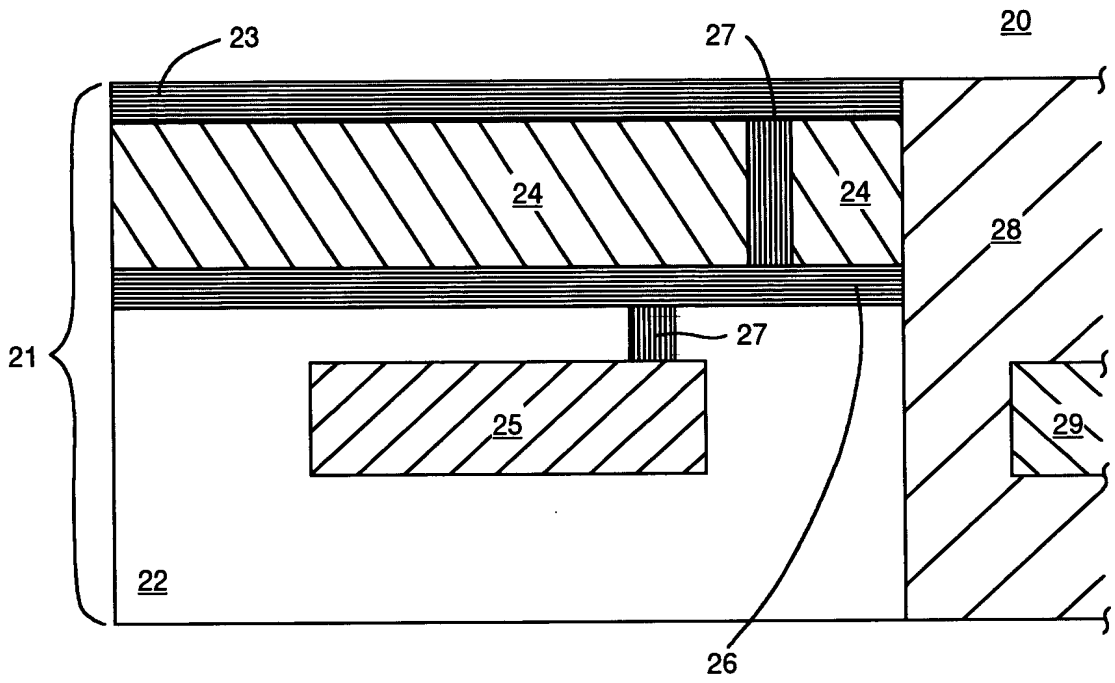
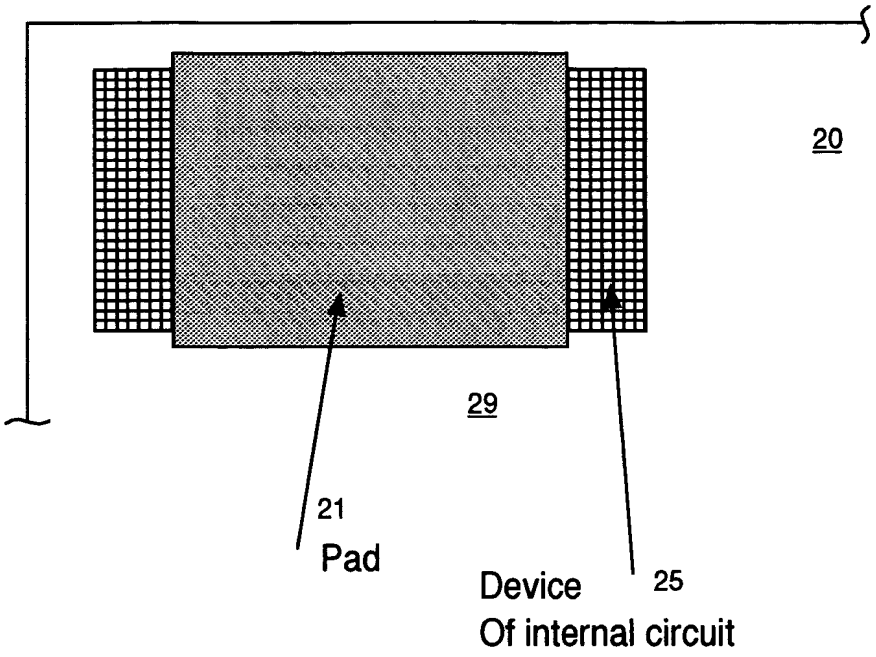
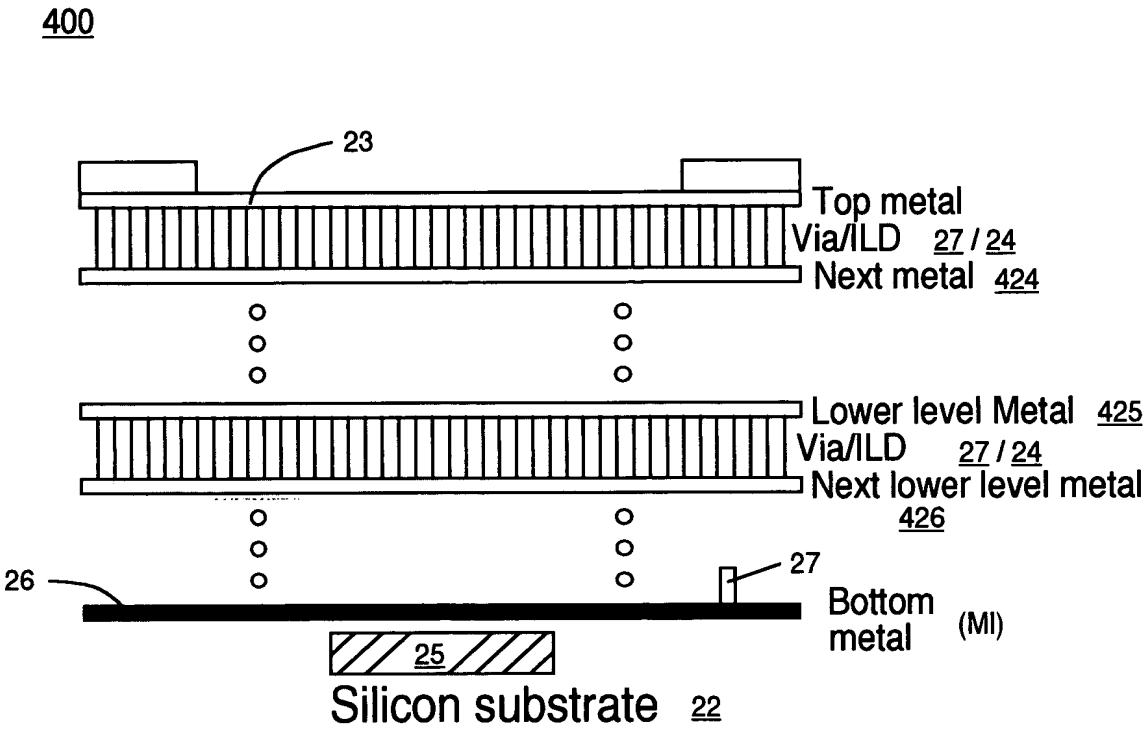


Fig. 2



Top side view

Fig. 3



Cross section view

Fig. 4

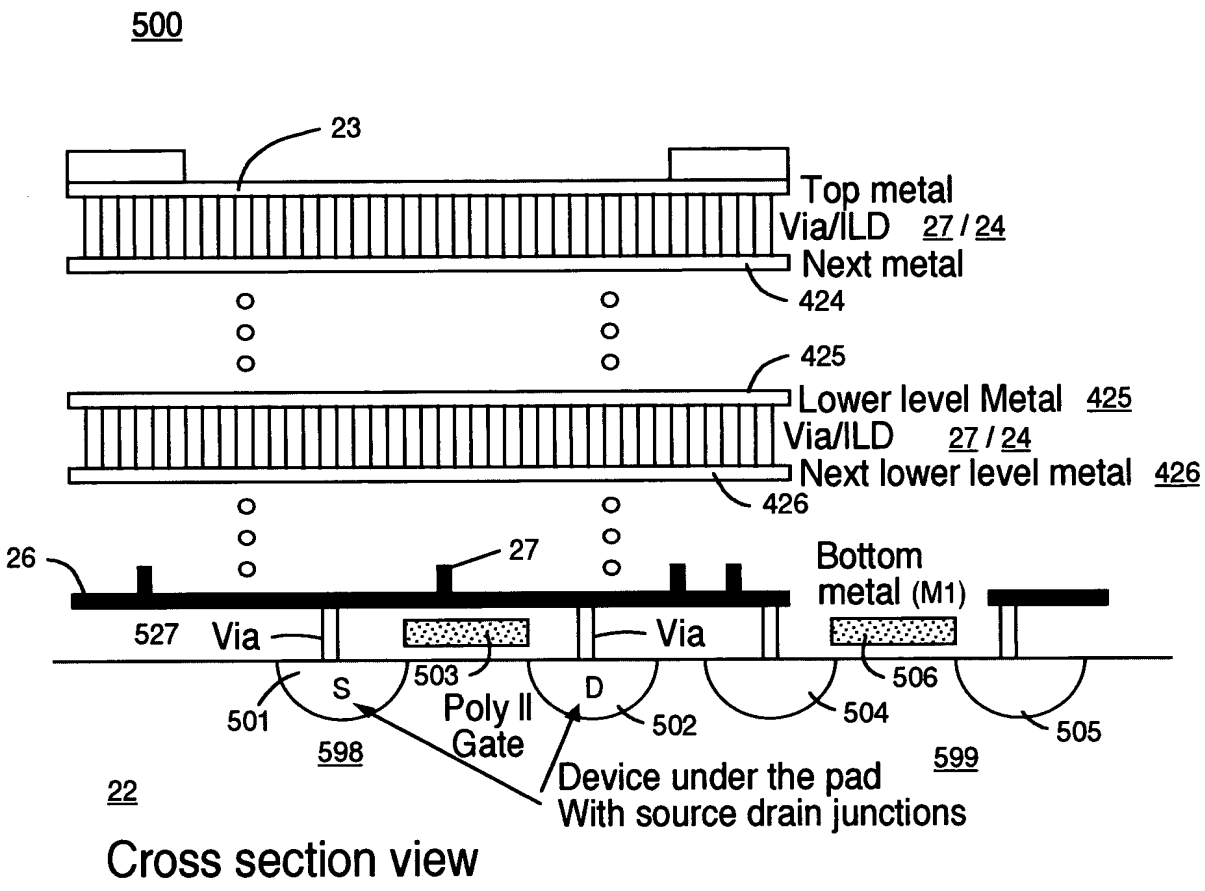

500
23
Top metal
Via/ILD 27 / 24
Next metal
424
425
Lower level Metal 425
Via/ILD 27 / 24
Next lower level metal 426
426
26
27
Bottom metal (M1)
527 Via
Via
503
506
S
D
501
Poly II Gate
502
504
505
598
599
22
Device under the pad With source drain junctions
Cross section view

Fig. 5

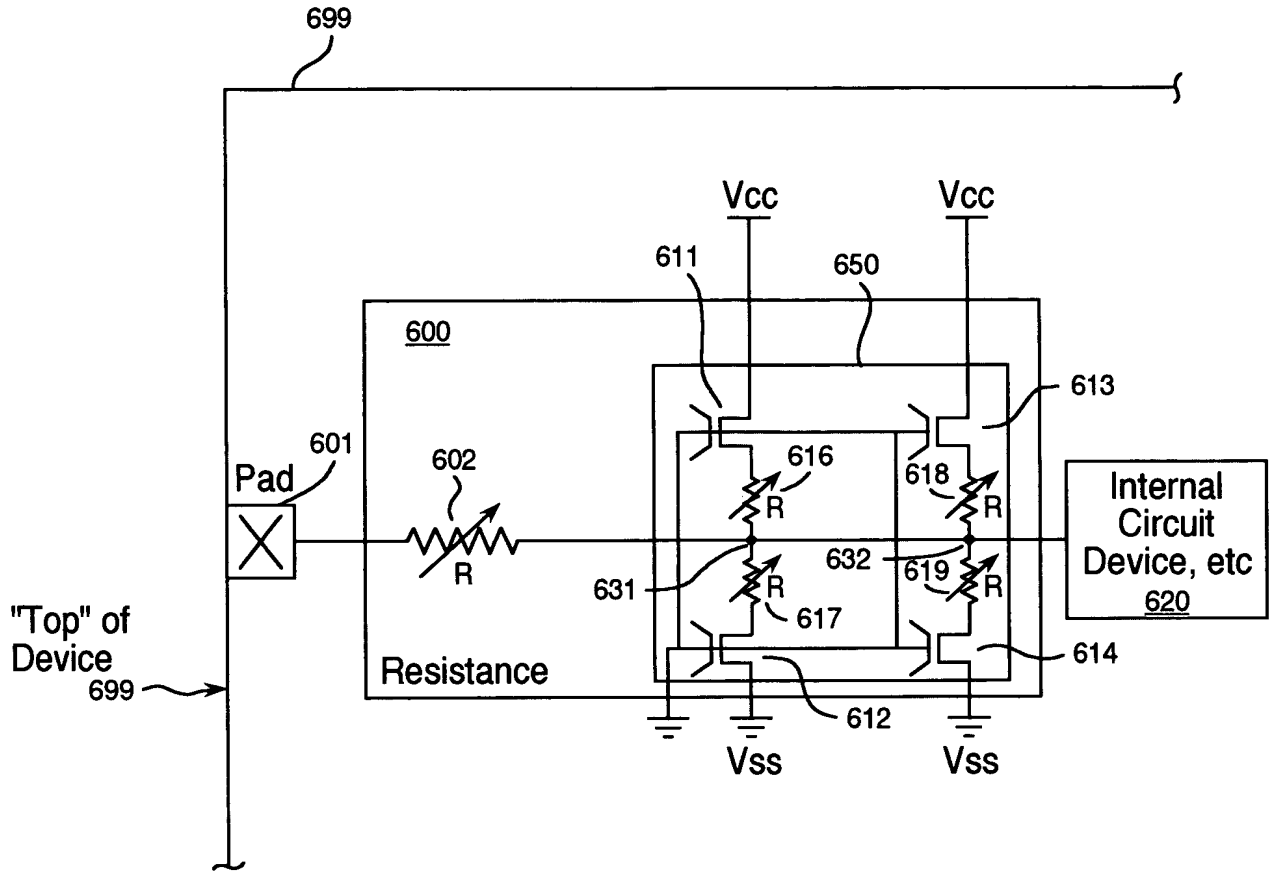

699
Vcc
Vcc
611
650
600
613
601
Pad
602
616
618
R
R
R
Internal
Circuit
Device, etc
620
632
631
619
R
R
617
"Top" of
Device
699
Resistance
614
612
Vss
Vss

Fig. 6

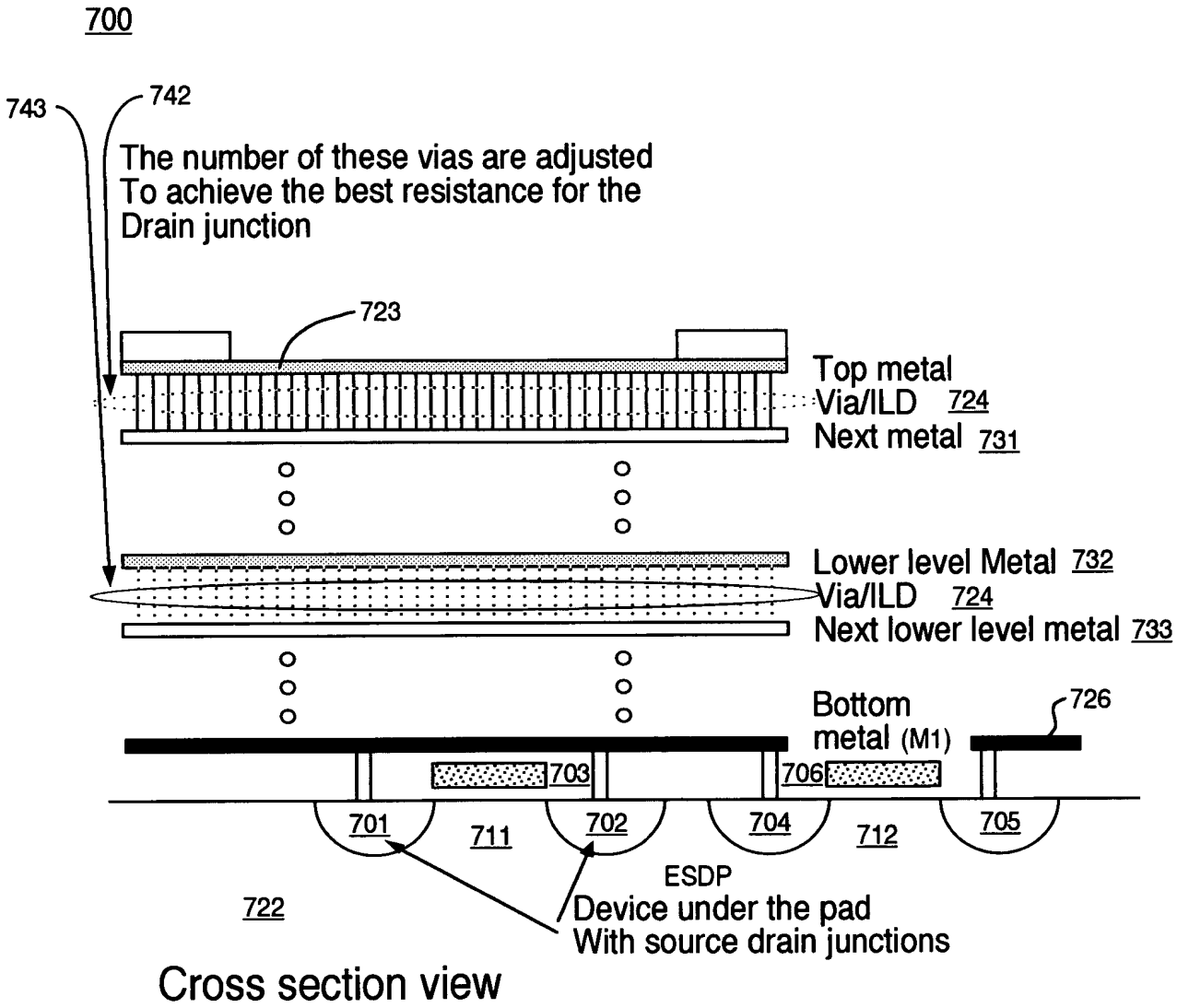

700
743
742
The number of these vias are adjusted
To achieve the best resistance for the
Drain junction
723
Top metal
Via/ILD 724
Next metal 731
Lower level Metal 732
Via/ILD 724
Next lower level metal 733
Bottom
metal (M1)
726
703
706
701
711
702
704
712
705
ESDP
722
Device under the pad
With source drain junctions
Cross section view

Fig. 7

80 Fabricating a Semiconductor Structure with ESD Protection

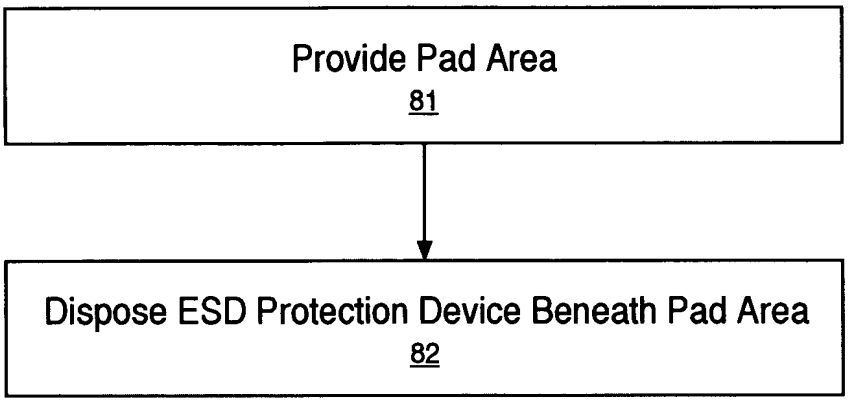


Fig. 8

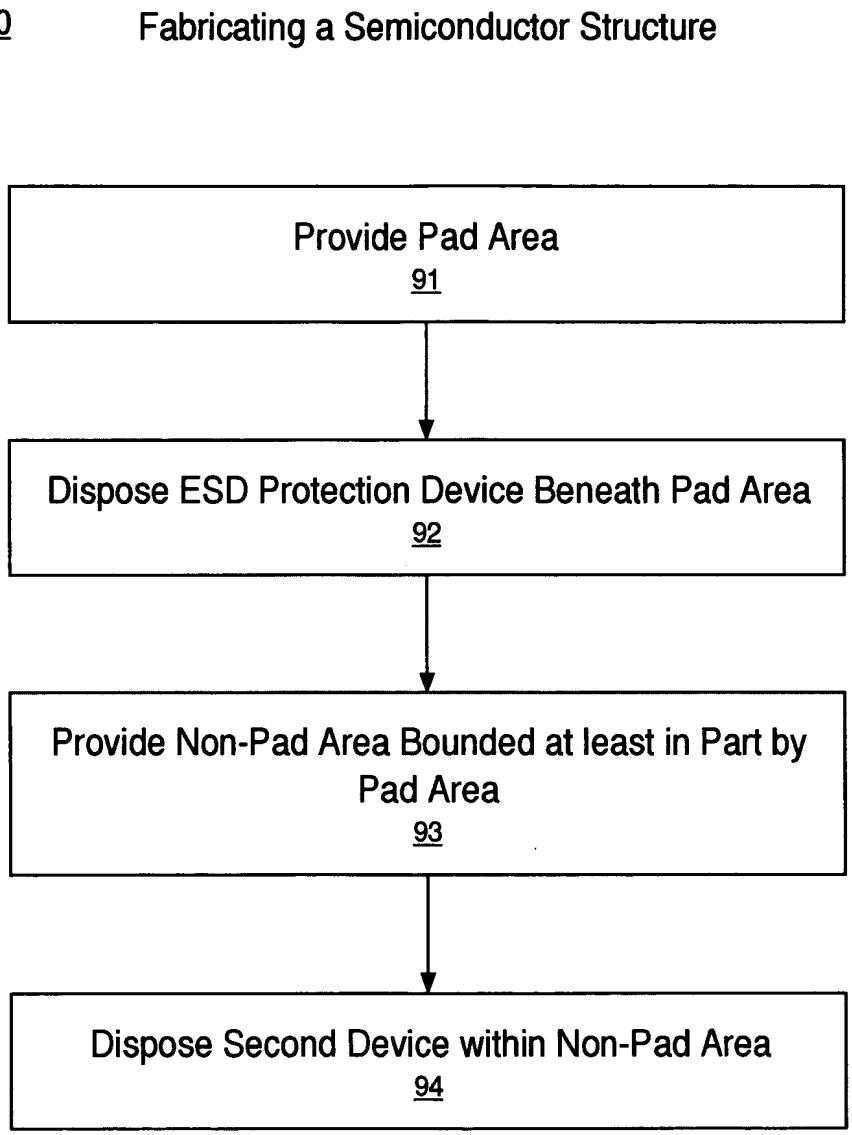

90
Fabricating a Semiconductor Structure
Provide Pad Area
91
Dispose ESD Protection Device Beneath Pad Area
92
Provide Non-Pad Area Bounded at least in Part by Pad Area
93
Dispose Second Device within Non-Pad Area
94

Fig. 9

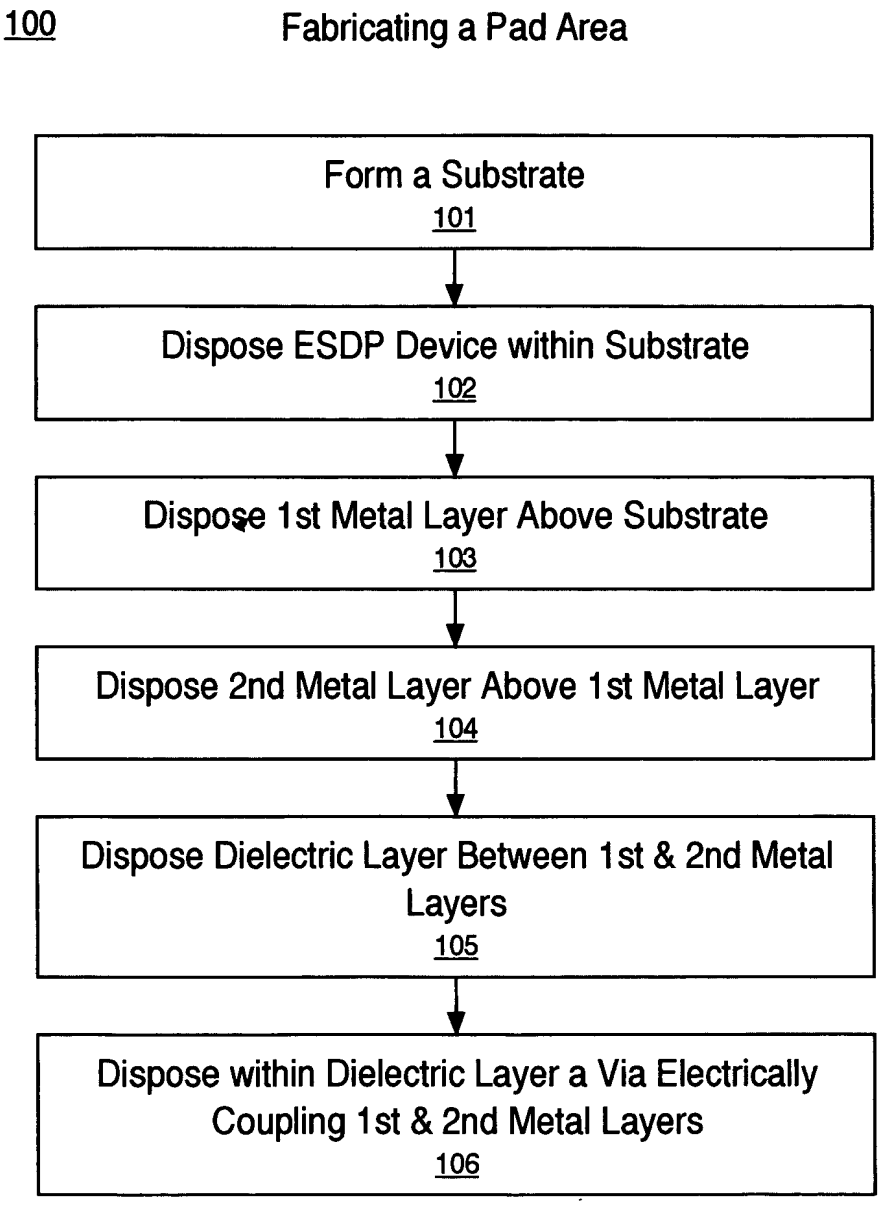

100
Fabricating a Pad Area
Form a Substrate
101
Dispose ESDP Device within Substrate
102
Dispose 1st Metal Layer Above Substrate
103
Dispose 2nd Metal Layer Above 1st Metal Layer
104
Dispose Dielectric Layer Between 1st & 2nd Metal Layers
105
Dispose within Dielectric Layer a Via Electrically Coupling 1st & 2nd Metal Layers
106

Fig. 10

1100 Fabricating a Pad Area with ESD Protection Device Below

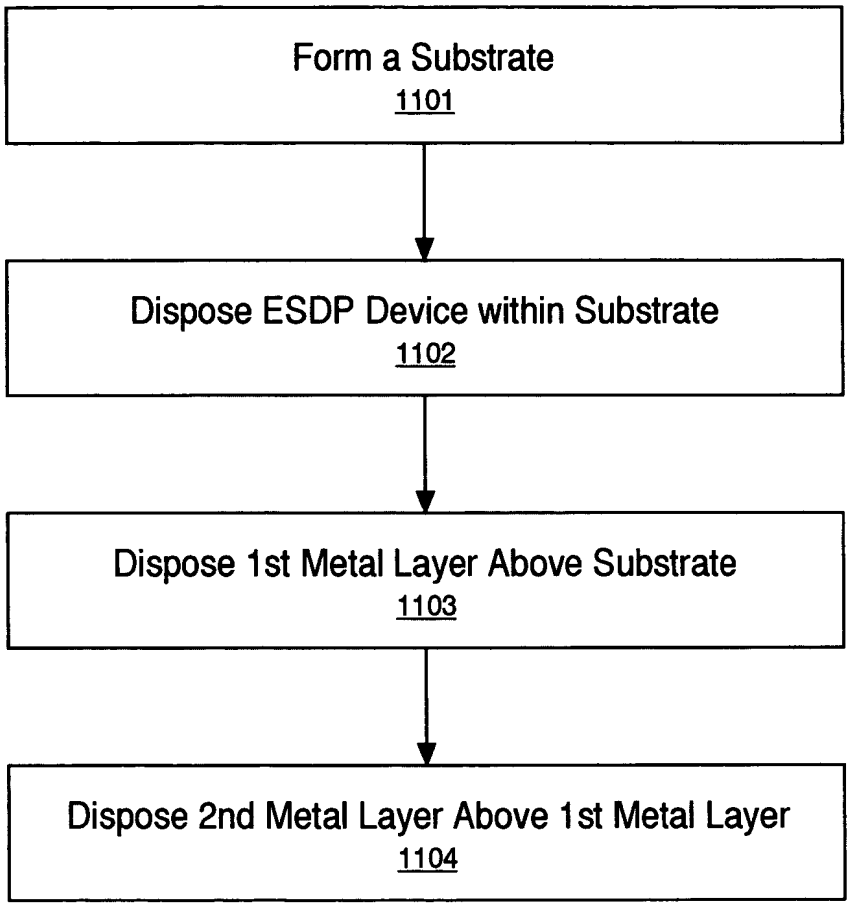


Fig. 11

1200 Fabricating a Pad Area with ESDP Below

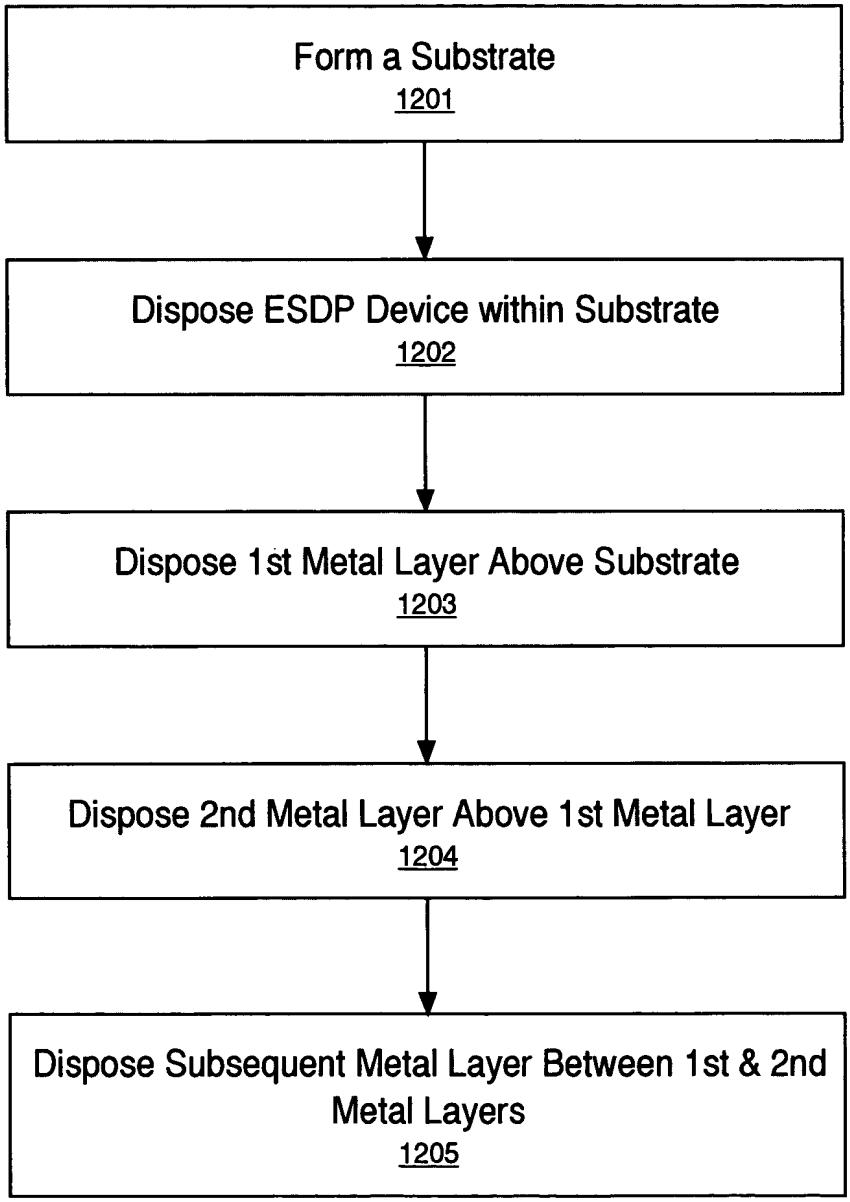


Fig. 12

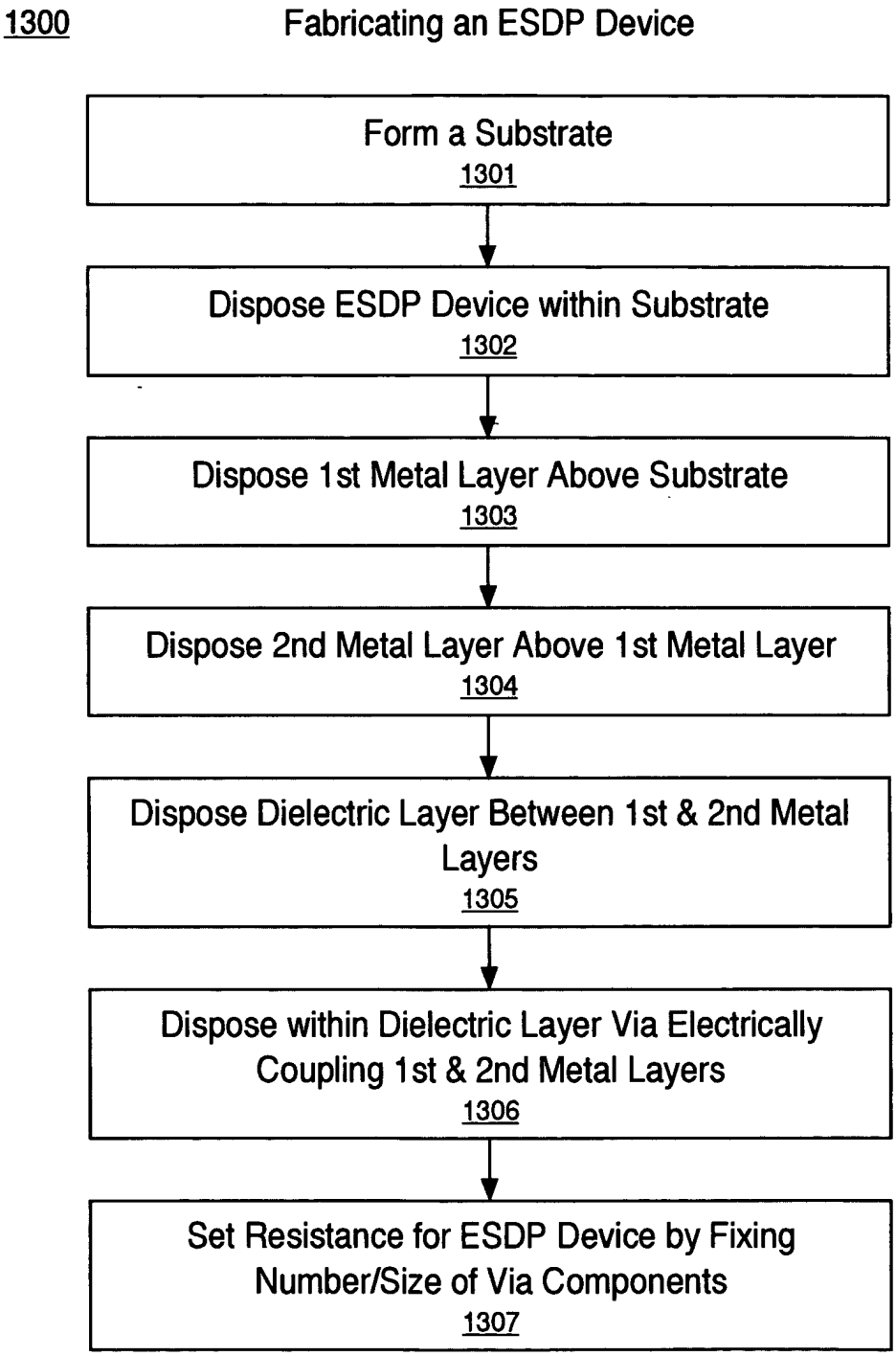

1300
Fabricating an ESDP Device
Form a Substrate
1301
Dispose ESDP Device within Substrate
1302
Dispose 1st Metal Layer Above Substrate
1303
Dispose 2nd Metal Layer Above 1st Metal Layer
1304
Dispose Dielectric Layer Between 1st & 2nd Metal Layers
1305
Dispose within Dielectric Layer Via Electrically Coupling 1st & 2nd Metal Layers
1306
Set Resistance for ESDP Device by Fixing Number/Size of Via Components
1307

Fig. 13